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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/879,208	06/13/2001	Yukihito Oowaki	02887.0141-01000	4453

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EXAMINER
RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/14/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/879,208	Applicant(s) Yokihito Oowaki et al.	
	Examiner Steven H. Rao	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3 and 101* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Priority

Receipt is acknowledged of paper submitted under 37 CFR 1.53 (b), which papers have been placed of record in the file, indicating that the instant application's claim to priority form U.S. Serial No. 09/340,149 , now U.S Patent No. 6,278,1650 has been granted.

Therefore claims 10 and 13 as originally recited and claims 11 and 12 as recited in the amendment of June 13, 2001 are currently pending in the application.

Continued Prosecution Application

The request filed on June 13, 2001 for a Divisional Application (Div.) under 37 CFR 1.53(b) based on parent Application No. 09/340149 is acceptable and a Div. has been established. An action on the Div. follows.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filed on June 13, 2001.

The references on PTO 1499 submitted on June 13,2001 are acknowledged. All the cited references have been considered and PTO 1449 initialed and the contract employees have been instructed to mail a copy of the initialed PTO-1449 to the applicants along with the Office Action.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed June 13, 2001.

Amendment to the specification page 12 lines 13-20 and claims 11 and 12 as set out in the preliminary have been entered and made of record in the file.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims as filed are replete with indefinite terms, phrases etc. which are too many to list them in full.

The following are the examples of indefinite terms, phrases etc.

Claim 10 line 4 , " top surfaces of said source/drain regions provided so as to sandwich said channel plane therbetween is elevated from said channel plane to be arranged toward said gate"

Claim 11, " laminating a semiconductor layer in said groove to polish top surfaces of said oxide film and said semiconductor film,"

Claim 12 lines 6-7, " which sandwich a region serving as a channel plane".

Applicants' cooperation is sought to correct the extensive errors in the claims.

The Office reserves the right to request substitute claims if these extensive errors are not corrected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 10 to the extent understood is rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (.U.S. Patent No. 5, 270, 257, herein after Shin).

With respect to claim 10, Shin describes a MIS transistor comprising a semiconductor substrate (Shin fig. 3a # 21, col. 4 line 19), source/drain regions (fig. 3c # 26 b (s) and 26 a (d) , col. 4 lines 46 and 47) formed on the substrate, a gate electrode (fig. 3b # 24 , col. 4 line 41) formed above a channel region (fig. 3 b region below gate 24 and oxide 23) between the source and drain regions, wherein the substantially flat top surfaces of the source/drain regions sandwich the channel plane there between and (flat top surfaces) are elevated from the channel plane (Shin fig. 3c) and an inclined surface formed between the level of the flat top surface of the source /drain and the level of the channel plane (fig. 3c), a gate insulator film (fig. 3c-e # 27-oxide) surrounding the gate and wherein the oxide in the upper side of the channel plane has T-shaped cross section and a lower side is tapered by a step portion (figs. 3 c-e) .

Claims 11-13 to the extent understood , are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (.U.S. Patent No. 5, 270, 257, herein after Shin) as applied to claim 10 above and further in view of Kirvokapic, U.S. Patent No. 6,025,635, herein after Kirvokapic).

With respect to claim11, Shin describes a method of making a MIS transistor comprising a semiconductor substrate (Shin fig. 3a # 21, col. 4 line 19), source/drain regions (fig. 3c # 26 b (s) and 26 a (d) , col. 4 lines 46 and 47) formed on the substrate, a gate electrode (fig. 3b # 24 , col. 4 line 41) formed above a channel region ((fig. 3 b region below gate 24 and oxide 23) between the source and drain regions the method including the steps of :

Selectively forming an oxide film (fig.3c # 23, col. 4 lines 30) on the semiconductor substrate.

Shin does not specifically describe the forming of a groove using the oxide as a mask .

However, Kirvokapic in fig.7 and col. 9 lines 14-16 describes of a groove using the oxide as a mask to accurately define and form the width of each device (Kirvokapic, col. 5 lines 5-10).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Kirvokapic's forming of a groove using the oxide as a mask for Shin forming of the groove after the oxide formation to accurately define and form the width of each device (Kirvokapic, col. 5 lines 5-10).

Further the steps of laminating a semiconductor layer in the groove to polish top surfaces of the oxide and semiconductor film (Kirvokapic fig. 11 3 240 , col. 6 lines 66-67) and remove the oxide film (Kirvokapic fig. 12 # 205, col. 7 line 4-5); using the semiconductor film as a mask to diffuse impurities to form grooved impurity diffusion region including bottom of the groove (Kirvokapic Fig. 12 , col. 6 line 39-42); arranging a high dielectric gate insulator film in a groove portion of the grooved impurity diffusion region so that a top surface of the gate insulator film is arranged farther from the semiconductor substrate than a top surface of the impurity diffusion region other than the groove portion (Kirvokapic fig. 12 # 205 , col. 7 lines 4-5) and forming a gate electrode on top of the gate insulator film. (Kirvokapic fig. 14 # 242).

With respect to claim 12, it repeats the steps of claim 11 and further additionally recites that the impurity diffused region is elevated from the channel plane formed on the surface of the semiconductor (Kirvokapic figs. 11 and 12 # 185 , col. 7 lines 8-20), forming an oxide on the side of the elevated region (Kirvokapic figs. 7 and 12 # 205, col. 6 line 11 and col. 7 line 4-5).

With respect to claim 13, in addition to the elements/steps recited in claim 11, claim 13 also recites the formation of an inclined surface between the top surface of the semiconductor layer and the channel plane.(KirvoKapic figs. 12 –15 # 245 and 250 forming an inclined surface between top surface of semiconductor 60 and channel plane region above/near 232).

Forming a dummy gate insulator film (Shin fig. 2a-b # 14, col. 2 line 51), and a dummy gate electrode having a second semiconductor layer on the channel (Shin fig. 2

a-b # 15, col. 2 line 55 bordering the first semiconductor layer by a lithography technique. (Shin col. 3 line 56), using the second semiconductor layer to diffuse impurity (Shin col.2 lines 60-63), removing dummy gate by etching (Shin col. 2 lines 64-65, fig. 2 c), depositing an insulator film to form a high dielectric gate insulator film in a groove portion of the grooved impurity diffusion region so that a top surface of the gate insulator film a gate insulator film (Shin fig. 3 b # 23, col. 4 line 30) and depositing a gate electrode on the entire top surface of the gate insulator film so as to have a grooved space at its center (Shin Fig. 3b # 24, col. 4 line 36) wherein the gate electrode has T-shaped cross section (Shin fig. 3c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is 703-306-5945. The examiner can normally be reached on M-F, 8.00 to 5.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703- 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703- 308-0956.

11/20/01

OLIK CHAUDHURI
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